What is claimed is:

1. A semiconductor memory device comprising:

a memory; and

a memory control circuit for controlling said memory, wherein:

said memory control circuit includes:

a bank busy circuit for variably setting a bank busy time that controls different bank cycle times;

a read data input circuit for inputting read data output from said memory in variable input timing;

a write data output circuit for outputting write data to said memory in variable output timing;

a command control circuit for issuing a command to said memory based on a memory command output from said bank busy circuit, thereby controlling different command interfaces;

a write mask circuit for controlling different write masks;

an initial sequence control circuit for controlling memories different in the initial sequence; and

an address generation circuit for controlling different address interfaces, and

said memory control circuit controls different memories using the same hardware.

2. The semiconductor memory device according to claim 1, wherein:

said bank busy circuit includes:

a program register for variably setting the bank

busy time; and

a bank busy counter for setting a value set on said program register, and then counting down the set value for each clock cycle when a bank n is accessed for turning on, and

said bank busy circuit provides said command control circuit with a memory command indicating cleared bank busy when the logic value of said bank busy counter becomes zero, thereby controlling memories different in the bank cycle time.

3. The semiconductor memory device according to claim 1, wherein:

said read data input circuit includes a first program register for variably setting the input timing of the read data output from said memory for controlling memories different in the access time, and inputs the read data output from said memory based on a set value on the first program register in variable input timing, and

said write data output circuit comprises a second program register for variably setting the output timing of the write data output to said memory, and adjusts the write data output timing based on a set vale on the second program register.

4. The semiconductor memory device according to claim 1, wherein said bank busy circuit switches the bank busy time using a switch.

5. The semiconductor memory device according to claim 1, wherein:

said write mask circuit relates to mask control for the write data output to said memory, and has a program register for switching between masking write operation using a Variable Write function when an FCRAM or an NWRAM is used, and masking the write operation using a Data Mask function when a DDR-SDRAM is used.

6. The semiconductor memory device according to claim 1, wherein:

said write mask circuit relates to mask control for the write data output to said memory, and has a switch for switching between masking of write operation using a Variable Write function when an FCRAM or an NWRAM is used, and masking of the write operation using a Data Mask function when a DDR-SDRAM is used.

7. The semiconductor memory device according to claim 1, wherein:

said address generation circuit relates to address generation of memories different in address assignment, and includes a program register for switching address generation logic.

8. The semiconductor memory device according to claim 1, wherein:

said address generation circuit relates to address generation of memories different in address assignment, and includes a switch for switching address generation logic.

9. The semiconductor memory device according to claim 1, wherein:

said initial sequence control circuit relates to

control of memories different in the initial sequence, includes a program register for variably changing the issue sequence of commands including mode register set, extension mode register set, auto refresh, and all bank pre-charge, and for variably changing set values on a mode register and an extension mode register, controls said memories different in the initial sequence using the same circuit, and issues an initial sequence command including the mode register set, the extension mode register set, the auto refresh, and the all bank pre-charge to said command control circuit.

10. The semiconductor memory device according to claim 1, wherein:

said initial sequence control circuit relates to control of memories having different initial sequences, includes a switch for variably changing the issue sequence of commands including mode register set, extension mode register set, auto refresh, and all bank pre-charge, and for variably changing set values on a mode register and an extension mode register, controls said memories different in the initial sequence using the same circuit, and issues an initial sequence command including the mode register set, the extension mode register set, the auto refresh, and the all bank pre-charge to said command control circuit.

11. The semiconductor memory device according to claim 1, comprising a power supply capable of adjusting a power supply output level supplied for said memory.

12. A mount-type semiconductor device for mounting said semiconductor memory device according to claim 1 on a

board, wherein:

said memory is different in the package size or the pin assignment, only the board for mounting the memory is changed, and one type of mother board is used for connecting the board for mounting the memory thereon when the memory different in the package size or the pin assignment is mounted.

13. A mount-type semiconductor device for mounting said semiconductor memory device according to claim 2 on a board, wherein:

said memory is different in the package size or the pin assignment, only the board for mounting the memory is changed, and one type of mother board is used for connecting the board for mounting the memory thereon when the memory different in the package size or the pin assignment is mounted.

14. A mount-type semiconductor device for mounting said semiconductor memory device according to claim 3 on a board, wherein:

said memory is different in the package size or the pin assignment, only the board for mounting the memory is changed, and one type of mother board is used for connecting the board for mounting the memory thereon when the memory different in the package size or the pin assignment is mounted.

15. The mount-type semiconductor device according to claim 12, wherein the board for mounting the memory thereon is a DIMM (Dual Inline Memory Module).

16. The mount-type semiconductor device according to claim 13, wherein the board for mounting the memory thereon is a DIMM (Dual Inline Memory Module).

17. The mount-type semiconductor device according to claim 14, wherein the board for mounting the memory thereon is a DIMM (Dual Inline Memory Module).

18. A mount-type semiconductor device for mounting said semiconductor memory device according to claim 1 on a board, wherein:

said memory is different in whether a terminating resistor is incorporated or not, and when the memory which is different in whether a terminating resistor is incorporated or not is mounted, a terminating resistor is not mounted on a DIMM (Dual Inline Memory Module) for the memory incorporating a terminating resistor, and a terminating resistor is attached to a DIMM for the memory not incorporating a terminating resistor, and one type of mother board is provided for connecting to the board for mounting the memory thereon.

19. A mount-type semiconductor device for mounting said semiconductor memory device according to claim 2 on a board, wherein:

said memory is different in whether a terminating resistor is incorporated or not, and when the memory which is different in whether a terminating resistor is incorporated or not is mounted, a terminating resistor is not mounted on a DIMM (Dual Inline Memory Module) for the memory incorporating a terminating resistor, and a

terminating resistor is attached to a DIMM for the memory not incorporating a terminating resistor, and one type of mother board is provided for connecting to the board for mounting the memory thereon.

20. A mount-type semiconductor device for mounting said semiconductor memory device according to claim 3 on a board, wherein:

said memory is different in whether a terminating resistor is incorporated or not, and when the memory which is different in whether a terminating resistor is incorporated or not is mounted, a terminating resistor is not mounted on a DIMM (Dual Inline Memory Module) for the memory incorporating a terminating resistor, and a terminating resistor is attached to a DIMM for the memory not incorporating a terminating resistor, and one type of mother board is provided for connecting to the board for mounting the memory thereon.